A Novel Cold-FET Method for Determining Extrinsic Capacitances Using a Capacitive Transmission Line Model

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***Abstract* — A novel cold-FET method using a capacitive transmission line (CTL) model to extract extrinsic capacitances for the small-signal equivalent circuit of field-effect transistors (FET's) is proposed. The extrinsic gate capacitance (C_{pg}) and drain capacitance (C_{pd}) of the FET's are extracted on the basis of the distributed CTL model and ABCD matrix representation for the depletion region beneath gate under the pinched-off cold-FET condition. The extraction method proposed is applied to obtain the small-signal equivalent circuit model for the FET's. The simulated *S* parameters using the CTL model exhibit great agreement with the measured *S* parameters.**

I. Introduction

The small-signal equivalent-circuit model plays an important role for evaluation of microwave performance of field-effect transistors (FET's) [1], [2] and design of monolithic microwave integrated circuits (MMIC's) [3]. The accurate extrinsic capacitance parameters are essential for determination of the small-signal equivalent circuit model [4], [5]. The pinched-off cold-FET methods [4]-[7], in which the gate voltage (V_{GS}) was biased to turn an FET off and the drain-to-source voltage (V_{DS}) was set to zero, have been widely studied to extract the extrinsic capacitance parameters of the FET's such as MESFET's, HFET's and HEMT's. These pinched-off cold-FET methods reported use lumped capacitance model to describe the intrinsic depletion region under the gate. The extrinsic gate capacitance (C_{pg}) and drain capacitance (C_{pd}) can be determined from the *Y*-parameter frequency response of the devices. On the other hand, the distributed capacitance model has been used to represent the intrinsic depletion region under the gate for the pinched-off cold FET to extract the C_{pg} and the C_{pd} [8]. The length of the depletion region was assumed to be linearly dependent on the gate bias. However, the assumption can not be applied to the common FET's with a uniformly-doped channel.

In this paper, we present a fast and simple method for extraction of extrinsic capacitances using a physically-meaningful capacitive transmission line (CTL) model and a linear regression technique [5]. The method developed provides an accurate technique for the small-signal equivalent circuit modeling of MESFET's, HFET's and HEMT's.

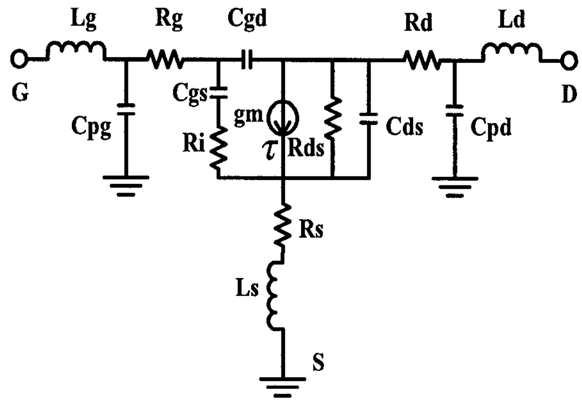

Fig. 1. Small-signal equivalent circuit of an FET.

II. Parameter Extraction

Fig. 1 shows the small-signal equivalent circuit of the FET's which consists of the intrinsic parameters (g_m, C_{gs}, C_{gd}, C_{ds}, R_i, R_{ds}, and τ) and the extrinsic elements (L_g, L_d, L_s, C_{pg}, C_{pd}, R_g, R_d, and R_s) [4].

On the basis of the equivalent circuit of Fig. 1, the small-signal equivalent-circuit model under the pinched-off cold-FET condition is proposed as shown in Fig. 2. The intrinsic depletion region of the pinched-off cold FET is described by the distributed CTL model which contains two kinds of the capacitances per unit length, the series capacitance (C_s) and the parallel capacitance (C_p). The ABCD matrix of the transmission line for the CTL model is indicated by M_{CTL} and expressed by [9]:

$$M_{\mathrm{CTL}} = \begin{bmatrix} cosh(\gamma l) & Z_0\, sinh(\gamma l) \\ \dfrac{sinh(\gamma l)}{Z_0} & cosh(\gamma l) \end{bmatrix} \tag{1}$$

where γ is the propagation constant, l is the length of the transmission line, and the Z_0 is the characteristic impedance. We have [8]

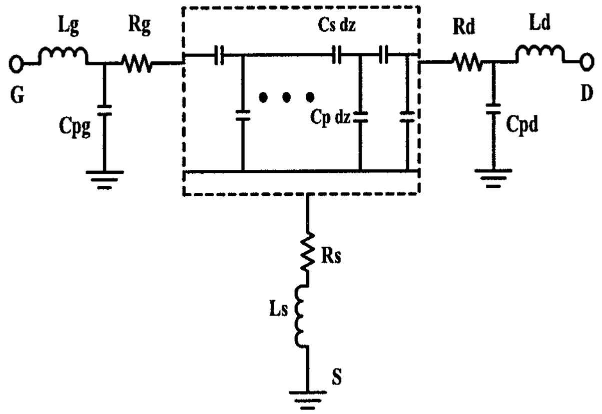

Fig. 2. Small-signal equivalent-circuit model of the pinched-off cold FET with the distributed CTL model for the intrinsic depletion region.

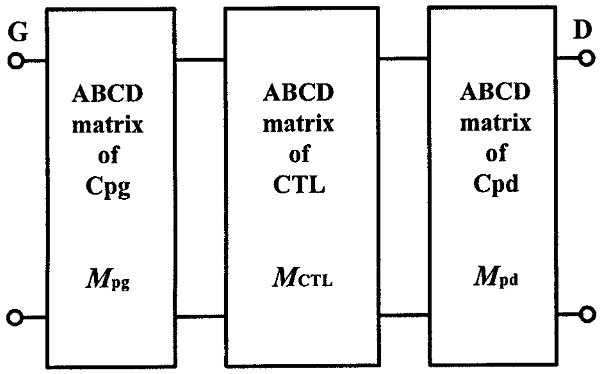

Fig. 3. Small-signal equivalent-circuit model of the pinched-off cold FET represented by the M_{CTL} in conjunction with the M_{pg} and the M_{pd}.

$$\gamma = \sqrt{\frac{C_p}{C_s}} \tag{2}$$

$$Z_0 = \frac{1}{j\omega\sqrt{C_p C_s}} \tag{3}$$

The small-signal equivalent-circuit model of the pinched-off cold FET can be represented by the Y parameters. The imaginary part of the Y parameters are not influenced by the extrinsic resistances (R_g, R_d, and R_s) and the extrinsic inductances (L_g, L_d, and L_s) at the frequencies up to a few GHz [4]. After ignoring the extrinsic resistances and inductances, the small-signal equivalent-circuit model of the pinched-off cold FET is described by the M_{CTL} matrix in conjunction with the ABCD matrices for the C_{pg} and the C_{pd} as shown in Fig. 3. The ABCD matrix of the C_{pg} is indicated by M_{pg} and that of the C_{pd} is indicated by M_{pd}. We get

$$M_{pg} = \begin{bmatrix} 1 & 0 \\ Y_{pg} & 1 \end{bmatrix} \tag{4}$$

$$M_{pd} = \begin{bmatrix} 1 & 0 \\ Y_{pd} & 1 \end{bmatrix} \tag{5}$$

where $Y_{pg} = j\omega C_{pg}$ and $Y_{pd} = j\omega C_{pd}$.

The ABCD matrix of the pinched-off cold FET is indicated by M_{FET} and expressed by

$$M_{FET} = M_{pg} \bullet M_{CTL} \bullet M_{pd} \tag{6}$$

The elements of the M_{FET} include

$$M_{FET11} = \cosh(\gamma l) + Y_{pd} Z_0 \sinh(\gamma l) \tag{7}$$

$$M_{FET12} = Z_0 \sinh(\gamma l) \tag{8}$$

$$M_{FET21} = (Y_{pg} + Y_{pd})\cosh(\gamma l) + \left(\frac{1}{Z_0} + Y_{pg} Y_{pd} Z_0\right)\sinh(\gamma l) \tag{9}$$

$$M_{FET22} = \cosh(\gamma l) + Y_{pg} Z_0 \sinh(\gamma l) \tag{10}$$

The M_{FET} is then transformed to the Y-parameter matrix, Y_{FET}. We have

$$Y_{FET11} = Y_{pg} + \frac{1}{Z_0 \tanh(\gamma l)} \tag{11}$$

$$Y_{FET22} = Y_{pd} + \frac{1}{Z_0 \tanh(\gamma l)} \tag{12}$$

The imaginary part of the Y_{FET} can be expressed by the following equations:

$$\frac{\mathrm{Im}(Y_{FET11})}{\omega} = C_{pg} + \frac{\sqrt{C_p C_s}}{\tanh(\gamma l)} \tag{13}$$

$$\frac{\mathrm{Im}(Y_{FET22})}{\omega} = C_{pd} + \frac{\sqrt{C_p C_s}}{\tanh(\gamma l)} \tag{14}$$

For a fixed pinched-off cold-FET bias, the C_p, C_s, γ, and l are constant.

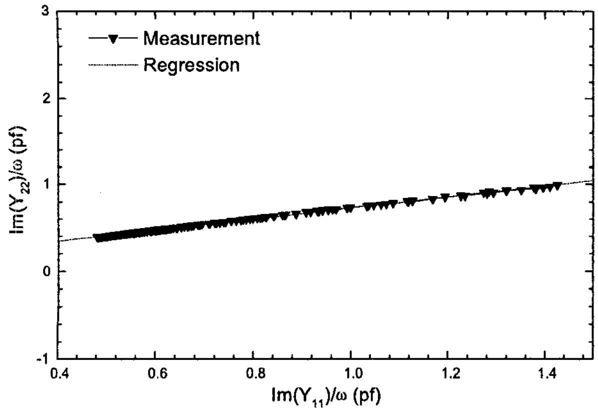

Fig. 4. Imaginary parts of measured Y_{22} parameters versus Imaginary parts of measured Y_{11} parameters represent the relationship between C_{pg} and C_{pd}.

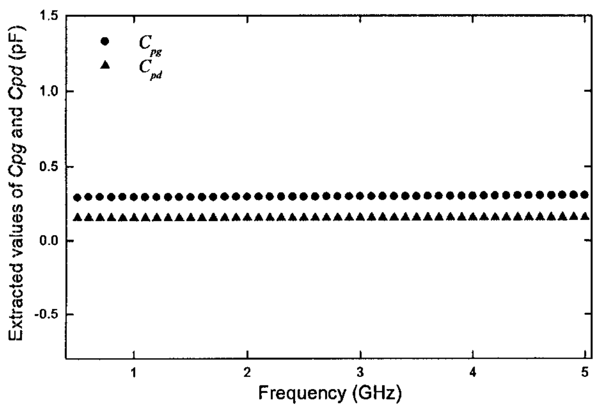

Fig. 5. Frequency response of the C_{pg} and the C_{pd}.

Fig. 4 shows the measurement characteristics of the $\mathrm{Im}(Y_{22})/\omega$ versus the $\mathrm{Im}(Y_{11})/\omega$ The $\mathrm{Im}(Y_{22})/\omega$ is linearly dependent on the $\mathrm{Im}(Y_{11})/\omega$. The slope of the $\mathrm{Im}(Y_{22})/\omega$ versus the $\mathrm{Im}(Y_{11})/\omega$ is obtained by the linear regression technique [5]. According to the slope value and the equations (13) and (14), we can determine the C_{pg} and the C_{pd}.

Fig. 5 shows the resulted frequency response of the C_{pg} and the C_{pd}. Both the C_{pg} and the C_{pd} are constant against frequencies. The extracted value of the C_{pg} is 0.299 pF and that of the C_{pd} is 0.154 pF.

III. Equivalent Circuit Model

The developed extraction method for the C_{pg} and C_{pd} can is to obtain the small-signal equivalent circuit model of the normally-operated FET. The element values of the small-signal equivalent circuit model for a submicron GaAs MESFET are extracted as follows: L_g=73.44 pH, L_d=71.31

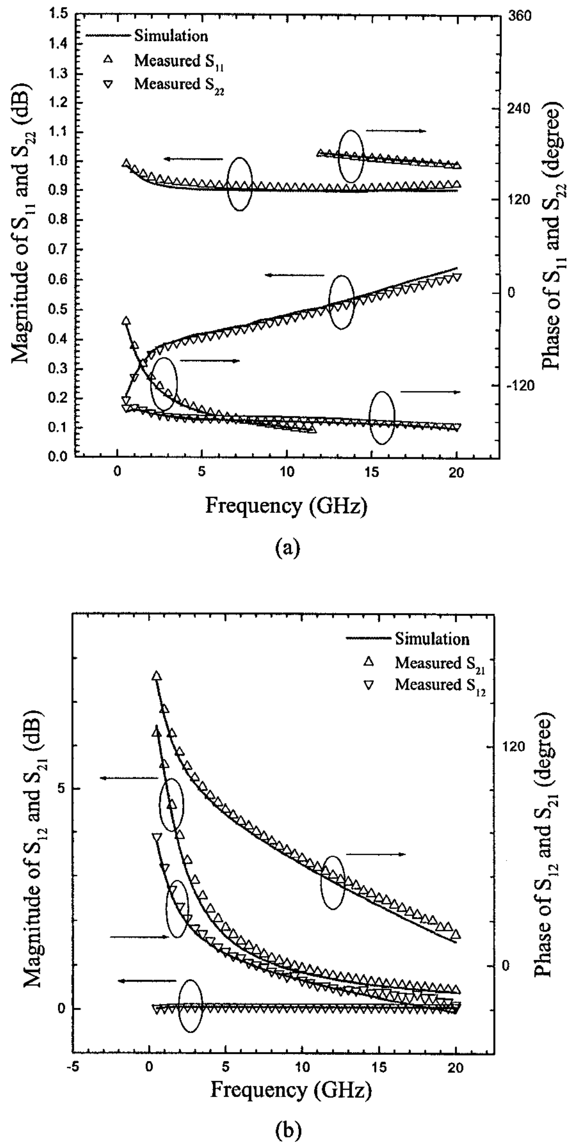

Fig. 6. Measured and Simulated S parameters. (a) S_{11} and S_{22} and (b) S_{12} and S_{21}.

pH, L_s=3.01 pH, C_{pg}=0.299 pF, C_{pd}=0.154 pF, C_{gs}=1.488 pF, C_{gd}=0.1717 pF, C_{ds}=0.0791 pF, R_g=0.35 Ω, R_d=0.48 Ω, R_s=0.46 Ω, R_i=2.075 Ω, R_{ds}=34.42 Ω, g_m=179 mS, τ=2.186 pS. Fig. 6 shows the simulated S parameters based on the extracted parameters of the small-signal equivalent circuit model in comparison with the measured S parameters. The excellent agreement between the simulated S parameters and the measured ones is demonstrated.

VI. Conclusion

The extrinsic capacitances, C_{pg} and C_{pd}, are extracted using a new pinched-off cold-FET method. The distributed CTL model is used to represent the intrinsic depletion region under the gate. The ABCD matrix representation is adopted for the equivalent circuit of pinched-off cold FET. The frequency response of the C_{pg} and the C_{pd} are determined according to the CTL model and the linear regression technique. The accurate small-signal equivalent circuit model for FET's is achieved by the proposed method.

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